Feature Extraction of Digital Aerial Images by FPGA based implementation of edge detection algorithms

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***Abstract*—Edge of image is one of the most fundamental and significant features. Edge detection is always one of the classical studying projects of computer vision and image processing field. It is the first step of image analysis and understanding. With the continuous improvement of remote sensing image, especially the appearance of Digital Aerial Image, edge detection is necessary step to extract information from the Digital Aerial images. .The purpose of edge detection is to discover the information about the shapes and the reflectance or transmittance in an image. The correctness and reliability of its results affect directly the comprehension machine system made for objective world. In this paper FPGA-based architecture for edge detection algorithms has been proposed. The implementation of edge detection algorithms on a field programmable gate array (FPGA) is having advantage of using large memory and embedded multipliers. FPGAs are providing a platform for processing real time algorithms on application-specific hardware with substantially higher performance than programmable digital signal processors (DSPs). The proposed architecture can be used as a building block of a aerial imaging systems for navigation and for the pattern recognition. The hardware implementation results are presented for the Sobel and Prewitt operator.**

***Keywords*—Edge detection algorithms; First gradient based operators; FPGA implementation; Prewitt operator; Sobel operators**

I. INTRODUCTION

In recent years, with the rapid development of economic, the process of town urbanization developed continuously, and land-use has becoming a community-wide hot issue. The construction land becomes increasingly tense and getting greater pressure. Therefore, extracting the current building information from high resolution image and getting the current land use have provided a guarantee for rational planning and utilization of land resources in villages and towns. With the rapid development of remote sensing technology, we can choose the present application of the high resolution remote sensing image, as well as the digital aerial image .

The emergence of digital aerial camera solves the problem of the low productivity of traditional image and the poor real-time photographing [1]. Compared with aerial film scanning digital image, digital aerial image have higher spatial resolution and geometric accuracy, rich in detailed texture information, and have the advantages of better real-time photographing and high efficiency. Building extraction in towns and villages based on the digital aerial image has important significance for dynamic monitoring on the village land-use. In image processing and computer vision. edge detection is a process which attempts to capture the significant properties of objects in the image. These properties include discontinuities in the photometrical, geometrical and physical characteristics of objects. Such information give rise to variations in the grey level image; the most commonly used variations are discontinuities (step edges), local extrema (lines edges), and 2D features formed where at least two edges meet (junctions) [2]. The purpose of edge detection is to localize these variations and to identify the physical phenomena which produce them. Edge detection must be efficient and reliable because the validity, efficiency and possibility of the completion of subsequent processing stages rely on it. To fulfill this requirement, edge detection provides all significant information about the image. The paper is organized as follow. The Edge detection algorithms are discussed in Section II and The hardware architecture of proposed model is presented in Sections III. The implementation details and results of different edge detection methods is given Section VI which is followed by the conclusions in Section V.

II. EDGE DETECTION ALGORITHMS

The Edge detection process detects outlines of an object and boundaries between objects and the background in the image. An edge-detection filter can also be used to improve the appearance of blurred or anti-aliased video streams. The basic edge-detection operator is a matrix area gradient operation that determines the level of variance between different pixels. Examples of gradient-based edge detectors are Roberts, Prewitt, and Sobel operators. All the gradient-based algorithms have kernel operators that calculate the strength of the slope in directions which are orthogonal to each other, commonly vertical and horizontal. Later, the contributions of the different components of the slopes are combined to give the total value of the edge strength. In the present work we present hardware implementation of Prewitt, and Sobel edge detection algorithm.

These algorithms consist in a 2-D first derivate operator applied to the grey-scale image to highlight regions of the image with high first spatial derivates. The edges are translated into ridges in the gradient magnitude of the image. The algorithm tracks along the top of these ridges and sets to zero all pixels that are not actually on the ridge top and give a thin line in the output. The edge detection of an image is the convolution products of the image pixels with different masks

which result in the calculation of the horizontal and the vertical gradient. The two gradients are calculated using differences between adjacent pixels. One way to find edges is to use the Prewitt kernels. The Prewitt kernels are based on the idea of the central difference, and are expressed by the following first order spatial derivates:

$$\frac{\partial I}{\partial x} \approx \frac{I(x+1,y)-I(x-1,y)}{2}$$

$$\frac{\partial I}{\partial y} = \frac{I(x,y+1)-I(x,y-1)}{2}$$

The two derivates correspond to a convolution kernel consisting in the horizontal convolution expressed by {-1,0,+1} and the vertical convolution expressed by {-1,0,1}. These convolutions are applied to the grey-scale image to get the horizontal (Kx) and the vertical gradients (Ky).

1	0	-1
1	0	-1
1	0	-1

(Kx)

1	1	1
0	0	0
-1	-1	-1

(Ky)

Fig.1 Prewitt Convolution Kernels

In order to perform the convolution on the entire image, the idea consists in building a n x n (typically 3 x 3) matrix of numbers called kernel mask, and in multiplying it with a portion of the image of the same dimension. Then, all the products are summed in order to determine the central pixel value. The kernel mask using Prewitt coefficients will be the matrix reported in (Kx) for the vertical edge detection and the one reported in (Ky) for the horizontal edge detection. The results of the convolution will stay in the range defined by the pixel resolution in number of bit, thus if the pixel resolution is 8 bits, the range of the results will be [0:255]. If a resulting pixel exceeds the range, it has to be normalized.

The Sobel algorithm is provides a differencing as well as noise smoothing operation in the single kernel. Thus, noise sensitivity of first gradient based operations can be avoided by the use of this algorithm. The vertical and horizontal kernels for the Sobel algorithm is given as.

1	0	-1
2	0	-2
1	0	-1

(Kx)

1	2	1
0	0	0
-1	-2	-1

(Ky)

Fig.2 Sobel Convolution Kernels

The vertical edge component is calculated with kernel Kx and the horizontal edge component is calculated with kernel Ky. |Kx| + |Ky| gives an indication of the intensity of the gradient in the current pixel. By using the threshold the effect of spurious noise in the extracted features can be reduced. With Sobel operator the lines corresponding to edges becomes thickens compared with the Roberts Cross and Prewitt operator output due to the increased smoothing of the Sobel operator.

Sobel and Prewitt operator are utilized extensively in the image processing for example in [4] Sobel edge detection is targeted for image processing and volume rendering applications. A CMOS 0.18um technology based Sobel processor was built as a part of the real-time shear-warp factorization volume rendering system to compute a gradient. In [5] A novel scheme combining Sobel technology with genetic algorithm is proposed to protect image copyright. For the Sobel-based copyright protection schemes in the literatures, they use Sobel technology to detect the edge of the cover image, i.e. the copyright image. In a method [6] proposed which combines Sobel edge detection operator and soft-threshold wavelet de-noising to do edge detection on images which include White Gaussian noises. In [7] a real-time algorithm to detect and track the target circle based on region growing In this paper, we proposed. The proposed algorithm consists of edge detecting, region growing, the possible centre of circle estimating and the centre of circle accurate locating in turn. It uses Prewitt operator to form the edge of image and divide the formed edge into different connected sub-region by region growing method.

In fact, Edge detector operators are two dimensional extension of the basic FIR filter. The FPGA architecture allows implementation of the algorithms with parallel architecture. the look up table (LUT) SRAM based on FPGA can offer a technology to realize the digital filters or other important digital signal processing by the distributed arithmetic (DA) technology conveniently[8]. Considering the advantages offered by the FPGA and relevance of Sobel and Prewitt algorithm we focus on FPGA implementation of the above two algorithms.

III. HARDWARE ARCHITECTURE FOR THE EDGE DETECTION

The hardware architecture is shown in the fig.3 .The proposed architecture consists of four major blocks. First the input pixels are passed through the Image delay line. Image delay line shifts the incoming image pixels through line buffers to create a delay line. Buffer depth depends on the number of pixels in each line. The number of buffer lines depends on the size of the convolution kernel. The pixels are forwarded to the vertical and horizontal kernel (Fig -1 and Fig-2). The kernel performs convolution operation with the pixels and the result of which is forwarded to the combining block .This block combines the results of horizontal and vertical convolution. The final out put of this block is the sum of the absolute values of the results of horizontal and vertical convolution.

The output of the combining block is the output of edge detection algorithm without the application of threshold

value hence it consist of some spurious noise. By controlling the threshold value in the Thresholding block the effect of noise can be reduced. Finally the output pixels are taken from the Thresholding block.

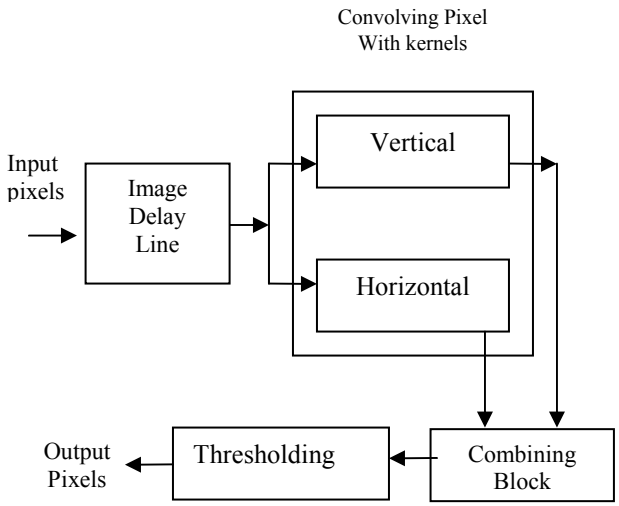


Fig.3 Hardware Architecture of the proposed system

IV. IMPLEMENATION DETAILS AND RESULTS

For FPGA implementation of the proposed architecture high level synthesis approach is taken. The proposed system is designed, implemented and verified using System generator. System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink® design environment for FPGA design. Previous experience with Xilinx FPGAs or RTL design methodologies are not required when using System Generator. Designs are captured in the DSP friendly Simulink modeling environment using a Xilinx specific blockset. All of the downstream FPGA implementation steps including synthesis and place and route are automatically performed to generate an FPGA programming file[9].

First of all using the Matlab the colored aerial images are converted to the gray scale images. The two dimensional image is converted in the one dimensional array. This value is passed to the system generator model from the work space.Figure.4 shows the system generator model of the image delay line for the 640X480 resolution image. Between first and second and second and third delay line output there is delay of 640 unit. First and third delay line have two unit delay additional which makes a pixel matrix of 3X3 to be available for the convolution with the Prewitt or Sobel kernels.

Figure 5. and 6 shows vertical and horizontal kernels for the Prewitt filter. As shown in the fig. 1 the values present in the Prewitt kernel are 1,-1 and 0 hence this structure do not require any multiplier. The kernel of Sobel operator have 2 and -2 as the one of the values .The multiplication by two can be achieved by simply a right shift operation. As can be seen that only digital blocks used in these kernels are adder subtracted tree , comparator and multiplexers. The output of these two blocks is 11 bit in the case of Prewitt edge detection and 12 bit in the case of Sobel edge detection.

The output vertical and horizontal kernels are the absolute values. As shown in figure 6. These values are passed to the combining block which is 11 bit in the case of Prewitt edge detection and 12 bit in the case of Sobel edge detection. Using the Slice block of System generator the output is truncated for the first 8 MSB bits. The Thresholding unit is shown in the square box in the figure.6. It consists of comparator and a multiplexer. Whenever the output of combining unit is more the threshold value 255 is generated as the output else 0 is generated as the output. The final results are stored in one Matlab variable and with the help of script it is displayed on the matlab environment. The design is implemented on the Virtex-4 DSP development kit with xc4vsx35-10ff668 FPGA on board. The operating clock rate for the design is 100MHz and it is able to produce the output in the .003 seconds.

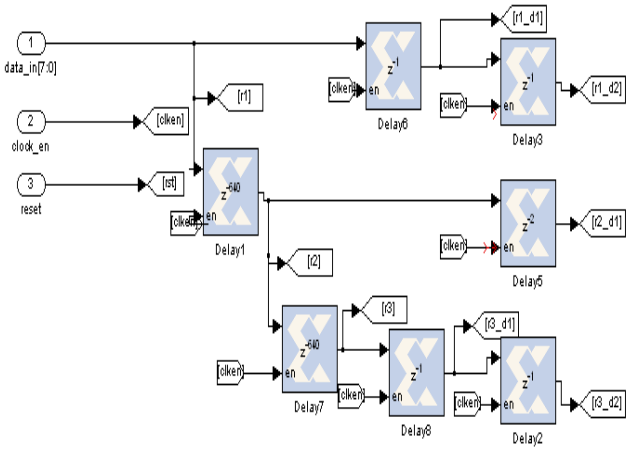


Fig.4 Implementation of the Image delay line

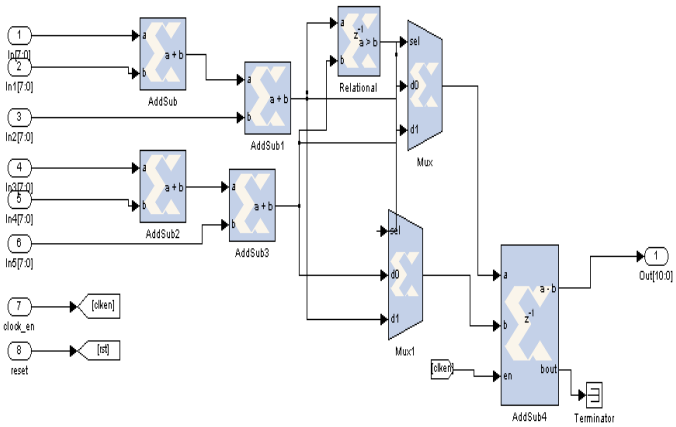


Fig.5. Implementation of the Vertical Kernel

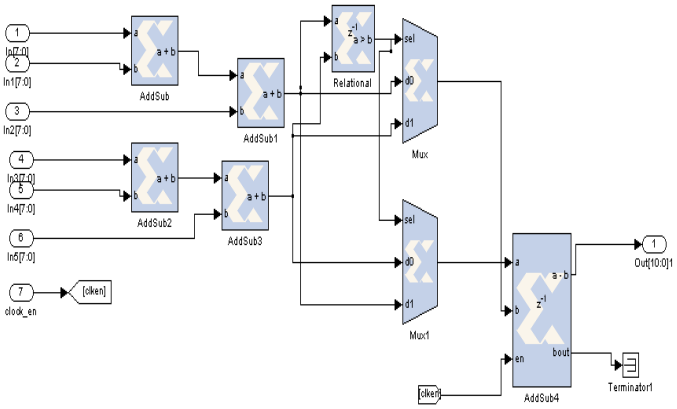


Fig.6 Implementation of the Horizontal Kernel

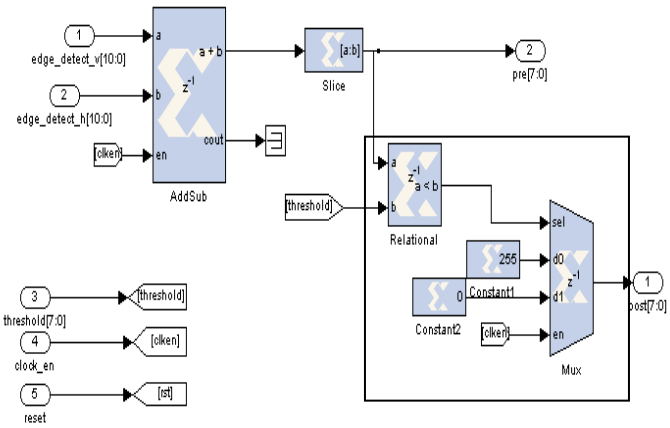


Fig.7 Implementation of the Combining and Thresholding unit

Figure 8 shows the original color aerial image, which is chosen as the test image, its gray scale conversion Figure 9(a) shows the output of the prewitt operator before and 9(b) after the application of the threshold values. We can note down the absence of the spurious noise at the post thresholding output.

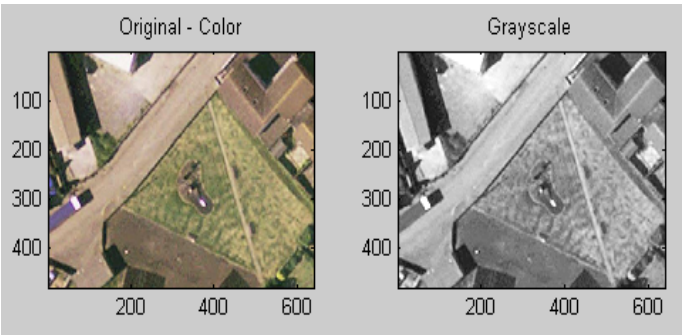
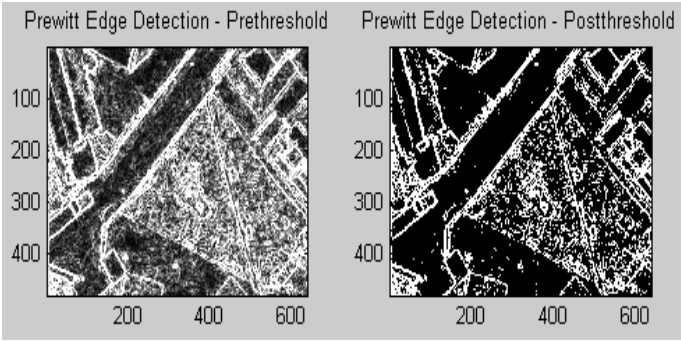


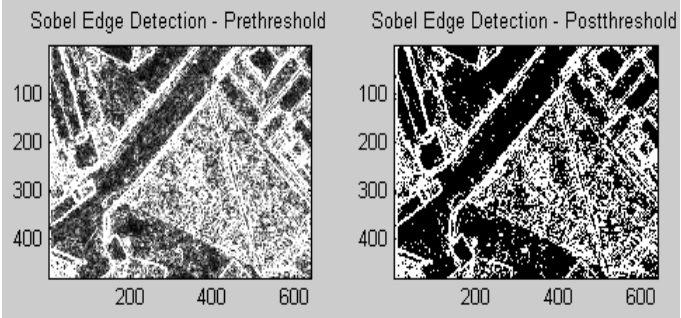
Fig.8 Original color aerial image and its grayscale version.



(a) (b)

Fig.9 Prewitt edge detector output

Figure 10(a) shows the output of the prewitt operator before and 10(b) after the application of the threshold values. We can note down the absence of the spurious noise at the post thresholding output as well as the thickness of the edges is more compared to the prewitt edge detector it is due to smoothening effect of Sobel edge detector.



(a) (b)

Fig.9 Sobel edge detector output

Table 1. shows the resource utilization summary. As shown the proposed approach is multiplier free so it consumes less area an less power. The higher number of Look-up- table utilizations are due to the implementation of delay line.

Table 1. Resource utilization summary

SN	Resource	Numbers
1.	Slice	451
2.	Flip flops	718
3.	LUT	850
4.	IOBs	58

V. CONCLUSION

In this paper two different methodologies for the edge detection of aerial images are implemented on the FPGA. Lower requirements of the FPGA resources make this method easy to be integrated with the aerial surveillance instruments and automatic navigation equipments.

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